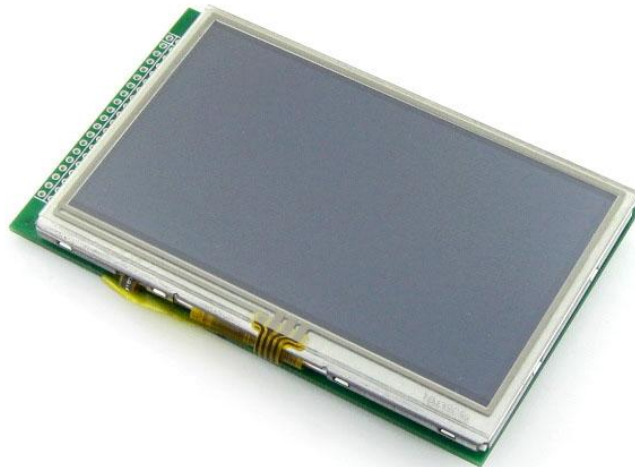


# 4.3inch 480x272 Touch LCD (A) User Manual



Chinese website: [www.waveshare.net](http://www.waveshare.net)

English Website: [www.wvshare.com](http://www.wvshare.com)

Data download: [www.waveshare.net/wiki](http://www.waveshare.net/wiki)

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# 1. Overview

Here are the main parameters of the LCD.

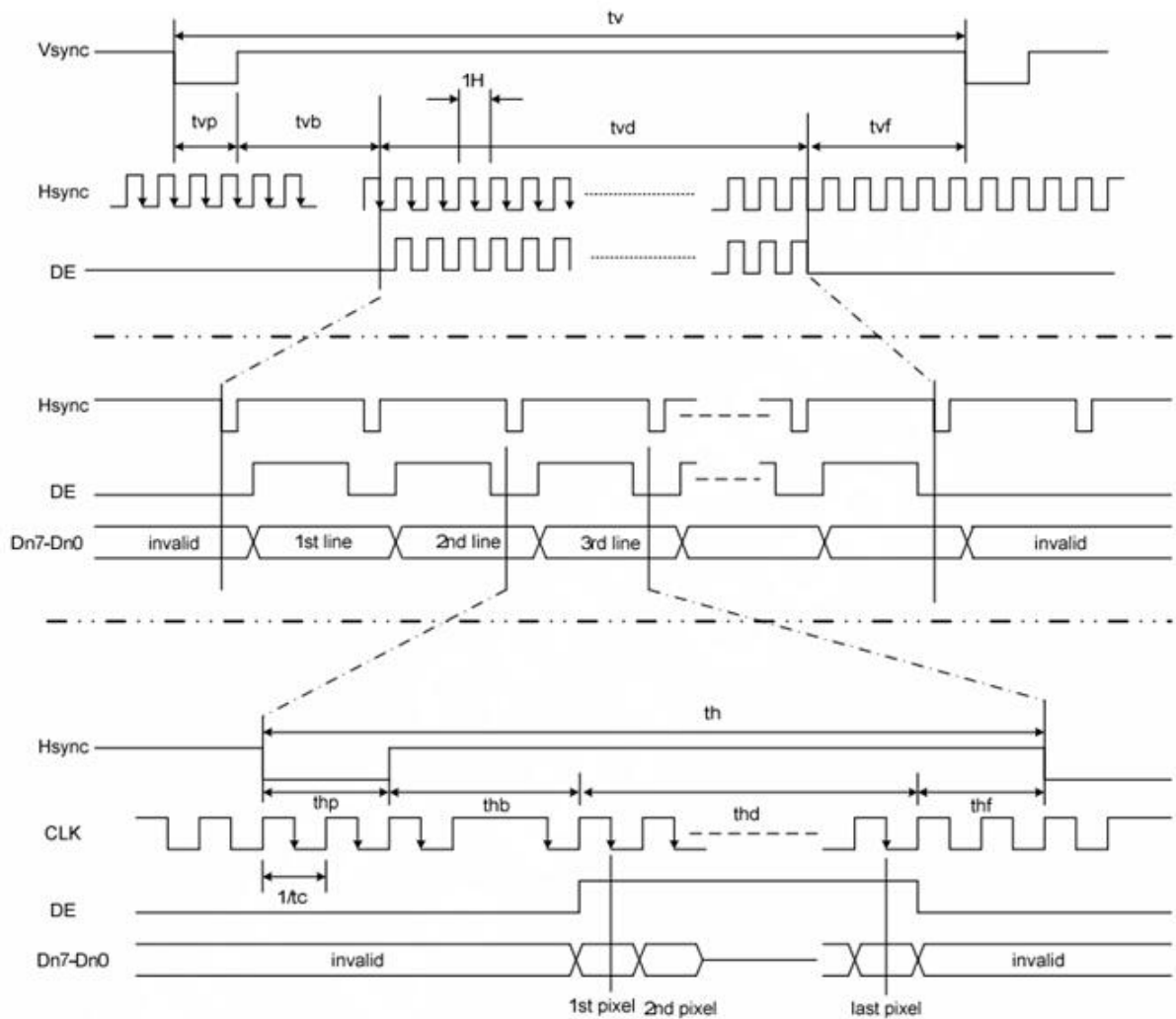
Module Type	TFT
Interfaces	LCD: 24-bit parallel RGA data input; Touch panel: 4-wire resistive touch screen
Backlight	LED
Response time (ms)	30
Contrast	500:1
Brightness(cd/m)	280
Display area(mm)	95.04(W)×53.86(H)
Dot pitch (mm)	0.006(W)×0.198(H)
Chromatic index	16,777,216
Aspect ratio	16:9
Resolution	480 X 272 (Pixel)
Power Dissipation	56mW
Back facet current	20mA
Operating temperature(°C)	-20 ~ +70

## 1.1 HX8257-A

HX8257-A is a TFT LCD single chip digital driver with features below:

- Support 480RGBx272 or 480RGBx240 graphics display TFT LCD panel;
- Support 8-bit serial RGB data and 24-bit parallel RGB data input;
- Power supply VDD: 1.8V~3.6V;
- 720-channel source outputs and 544-channel gate outputs;
- PWM control function to generate power for backlight.

When applying HX8257-A, a MCU with LCD controller is required, since the LCD controller is not included in this LCD. Here is the basic sequence of HX8257-A:



Pin descriptions:

Symbol	Description
Vsync	Vertical sync signal, which indicates the starting to scan a new frame. One frame refers to one picture shown in the LCD
Hsync	Horizontal sync signal, which indicates the starting to scan a new line
DE	Input data enable control
CLK	LCD clock
Dn7-Dn0	Parallel data

Here are the meanings of the symbols in the sequence diagram:

Symbol	Description	Reference			Unit
		Min.	Typ.	Max.	
fclk	LCD clock cycle	-	9	15	MHz
Horizontal signal					
th	Horizontal cycle	525	525	605	CLK <sub>(1)</sub>

thd	Horizontal display period	480	480	480	CLK <sub>(1)</sub>
thf	Horizontal front porch	2	2	82	CLK <sub>(1)</sub>
thp <sub>(2)</sub>	Horizontal pulse width	2	41	41	CLK <sub>(1)</sub>
thb <sub>(2)</sub>	Horizontal back porch	2	2	41	CLK <sub>(1)</sub>
<b>Vertical signal</b>					
tv	Vertical cycle	285	286	399	H <sub>(1)</sub>
tvd	Vertical display period	272	272	272	H <sub>(1)</sub>
tvf	Vertical front porch	1	2	227	H <sub>(1)</sub>
tvp <sub>(2)</sub>	Vertical pulse width	1	10	11	H <sub>(1)</sub>
tvb <sub>(2)</sub>	Vertical back porch	1	2	11	H <sub>(1)</sub>

Remarks:

- (1) Unit: CLK=1/f<sub>CLK</sub>, it is the duration for scanning a pixel; H=th, it is the duration for scanning a line;
- (2) It is necessary to keep tvp+tvb=12 and thp+thb=43 in sync mode. DE mode is unnecessary to keep it.

From the figure above, we can learn that:

The total time for scanning a line is: th = thp + thb + thd + thf; in the period of thd, when a clock plus comes, a pixel data will be transmitted via the parallel data interface. And there are 480 pixels each line for this LCD, so thd=480;

The duration for scanning a frame is: tv = tvp + tvb + tvd + tvf; Hsync can be regarded as the clock of vertical signals. A clock cycle of Hsync refers to the duration for LCD displaying a line. When a falling edge comes in Hsync, a new line will be displayed in the LCD. However, the actual data transmission only occurs in the period of tvd. And the LCD will display the new line in this case. There are 272 lines for this LCD, so tvd = 272.

Other parameters can be modified as required, according to the specifications listed in the tables above.

## 2. Hardware description

Pin No.	Symbol	Descriptions	I/O	Functions
1	5V	5V power supply	I	Supply 5V power voltage
2				
3	B0	Data line	I	Blue pallet data line
4	B1			
5	B2			

6	B3			
7	B4			
8	B5			
9	B6			
10	B7			
11	GND	Ground	I	GND
12	G0			
13	G1			
14	G2			
15	G3			
16	G4	Data line	I	Green pallet data line
17	G5			
18	G6			
19	G7			
20	GND	Ground	I	GND
21	R0			
22	R1			
23	R2			
24	R3			
25	R4	Data line	I	Red pallet data line
26	R5			
27	R6			
28	R7			
29	GND	Ground	I	GND
30	BL_EN	Backlight enable	I	1: Backlight ON 0: Backlight OFF
31	PWM	Backlight brightness control	I	Signal line for PWM control backlight
32	NC			
33	DE	Input data enable control	I	DE=0: SYNC mode DE=1: DE mode
34	VSYNC	Horizontal synchronization	I	Horizontal sync signal input
35	HSYNC	Vertical synchronization	I	Vertical sync signal input
36	DCLK	LCD clock	I	LCD clock signal source
37	Y+	Touch panel Y+	O	Resistive touch panel Y+ analog output
38	Y-	Touch panel Y-	O	Resistive touch panel Y- analog output

39	X+	Touch panel X+	O	Resistive touch panel X+ analog output
40	X-	Touch panel X-	O	Resistive touch panel X- analog output

4.3inch 480x272 Touch LCD (A) and 4.3inch 480x272 Touch LCD (B) share a same design of PCB. The differences between them are the parts on the boards and the way to lead out the pins. For 4.3inch 480x272 Touch LCD (A), its pins are led out with the FFC cable, including the pins Y-,Y+,X- and X+, and no touch chip is integrated on the board. For 4.3inch 480x272 Touch LCD (B), its pins are led out via the pin headers, and there is a touch chip XPT2046 integrated on the board.

### 3. Dimensions

